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APPLICATION

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TITLE: HIGH SPEED DIGITAL TO ANALOG CONVERTER USING MULTIPLE STAGGERED SUCCESSIVE APPROXIMATION CELLS

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HIGH SPEED DIGITAL TO ANALOG CONVERTER USING MULTIPLE STAGGERED SUCCESSIVE APPROXIMATION CELLS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from provisional application No. 60/243,324 filed October 25, 2000.

BACKGROUND

[0002] The basic operation of a CMOS active pixel sensor is described in U.S. patent No. 5,471,215. This kind of image sensor, and other similar image sensors, often operate by using an array of photoreceptors to convert light forming an image, into signals indicative of the light, e.g. charge based signals. Those signals are often analog, and may be converted to digital by an A/D converter. Image sensors which have greater numbers of elements in the image sensor array may produce more signals. In order to handle these signals, either more A/D converters must be provided, or the existing A/D converters need to digitize the data from these image sensors at higher signal rates. For example, a high precision CMOS active pixel sensor may require an A/D converter which is capable of 10 bits of resolution at 20 Megasamples per second.

[0003] Image sensors of this type are often limited by the available area or "real estate" on the chip, a and the available power for driving the chip. An advantage of using CMOS circuitry is that power consumption of such a circuit may be minimized. Therefore, the power consumption of such a circuit remains an important criteria. Also, since real estate on the chip may be limited, the number of A/D converters and their size should be minimized.

[0004] A/D converters with this kind of resolution, in the prior art, may have a power consumption of about 25 mW using a 3.3 volt power supply.

SUMMARY

[0005] The present application describes a system, and a special A/D converter using individual successive approximation A/D converter cells which operate in a pipelined fashion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] These and other aspects will now be described in detail with reference to the accompanying drawings, wherein:

[0007] Figure 1 shows a block diagram of a circuit on a chip including an image sensor and A/D converter;

[0008] Figure 2 shows relative timing of A/D converter cells;

[0009] Figure 3 shows an embodiment with built-in calibration in the system;

[0010] Figures 4A and 4B show two alternative schemes for implementing the A/D converter timing and control.

DETAILED DESCRIPTION

[0011] According to the present system, a plurality of successive approximation A/D converter cells are provided. The embodiment recognizes that the pixel analog data is arriving at a relatively high rate, e.g. 20 Mhz. A plurality of A/D converters are provided, here twelve A/D converters are provided, each running at 1.6 megasamples per second. The timing of these A/D converters are staggered so that each A/D converter is ready for its pixel analog input at precisely the right time. The power consumption of such cells is relatively low; and therefore the power may be reduced.

[0012] In the embodiment, an A/D converter with 10 bits of resolution and 20 megasamples per second is provided that has a power consumption on the order of 1 mW. Twelve individual successive approximation A/D converter cells are provided. Each requires 600 ns to make each conversion.

Since twelve stages are necessary, the total data throughput equals twelve / 600 ns = 20 megasamples per second. Each successive approximation A/D converter requires 12 complete clock cycles to convert the 10 bit data. The first clock cycle samples the input data, then 10 clock cycles are used to convert each of the bits. A single clock cycle is used for data readout.

[0013] A block diagram is shown in figure 1. Figure 1 shows how a single chip substrate 100 includes a photo sensor array 110. Photosensor array 110 can be an array of, for example, photodiodes, photogates, or any other type of photoreceptors. The output 115 of the array 110 is coupled to a timing circuit 120 which arranges the data to be sent to the A/D converter array 130. The data is sent such that each A/D converter receives data at a different, staggered time.

[0014] Figure 2 shows how the timing and switching of the data is carried out. The input signals from the image sensor array 110 are staggered and provided to the A/D converters at different times, preferably one clock cycle apart. Figure 2 shows the relative timing of four of the twelve A/D converter cells. The first row 200 for example may represent the first A/D converter. Data that is input during cycle No. 1 is available at the output of the A/D

converter during cycle No. 12. Different data from different ones of the converters are output in each cycle.

[0015] Figure 3 shows a block diagram of each of the twelve A/D converter elements. The elements may operate using capacitors formed by a capacitor array 300. In this embodiment, unit cell capacitors are formed. The capacitor array 300 is formed, for example, of N different elements, each of which are identical. Matching each of these capacitors may ensure linearity. A switching element 310 may switch the capacitor combinations in the proper way to convert a specific bit. As conventional in a successive approximation A/D converter, different bits are obtained and output during different clock cycles. Hence the clock input at 315 may select the different bits which are used and may hence select the number of the capacitor elements which are used.

[0016] This system may adaptively assign the channels to A/D converters in a different way than conventional. Conventional methods of removing fixed patterned noise, therefore, might not be as effective. Therefore, it becomes important that these A/D converters have consistent characteristics. In this embodiment, calibration may be used to compensate for offsets between the comparators of the system.

[0017] Successive approximation A/D converters as used herein may have built-in calibration shown as elements 320. Any type of internal calibration system may be used.

[0018] The inventors also realize that comparator kickback noise may become a problem within this system. That comparator itself may produce noise which may affect the signal being processed. In this embodiment, a single preamplifier, here shown as a follower 330, is introduced between the signal and the comparator.

[0019] This system also requires generation of multiple timing and control signals to maintain the synchronization. Each successive approximation A/D converter requires about 20 control signals. The timing is offset for each of the twelve different A/D converters. Therefore, digital logic is used to replicate control signals after a delay.

[0020] In one embodiment, shown in figure 4A, a plurality of flip-flops, here D type flip-flops, are used to delay the respective signals. In figure 4A, the control signals showed as A in and B in are separately delayed using a series of flip-flops; with A in delayed by flip-flops 400,408, 409; and B in delayed by flip-flops 404, 421,422. For example, the control signal A in is delayed by flip-flop 400 to produce signal A1, line 405, which is the first control signal for the first A/D converter 402.

Similarly, the B in control signal is delayed by flip-flop 404 to produce the B1 control signal for the A/D converter 402. The A1 signal 405 also drives the input of the second D flip-flop 408. The output of flip-flop 408 similarly drives flip-flop 409 and the like. Each successive output such as 405 is then delayed by the next flip-flop 408, and used as the respective second control (here A2, B2) for the A/D converters.

[0021] Each cycle of the A/D converter may require finer timing than can be offered by a usual clock. Hence, the clock input 410 may be a divided higher speed clock.

[0022] Two D type flip-flops are required to delay each signal. Any signal which is only half a clock cycle in length may require falling edge flip-flops, in addition to the rising edge flip-flops, and may also require additional logic.

[0023] Figure 4B shows an A/D converter cell with a trigger signal that is staggered by one or two flip-flops according to the master clocks. All of the local control signals may be generated locally within the A/D converter. Delayed versions of the clock are still obtained. For example, the D. type flip-flops 450 produces a delayed version 452. Delayed version 452 triggers the next the flip-flop 454 to produce delayed version 456. Each of the

delayed versions, such as 452, is further processed by the logic block 460. Logic block for 60 outputs the two control signals A1 and B1. For example, the control signal A1 may be output directly, with control signal B1 being delayed by a series of logic gates or transistors. Since this system uses fewer flip-flops, and only a single input signal, it may allow for improved symmetry between the A/D converters.

[0024] Although only a few embodiments have been disclosed in detail above, other modifications are possible. For example, different logic techniques may be used herein. In addition, while the above describes specific numbers of bits, the same techniques are applicable to other numbers of elements. For example, this system may be used with as few as three elements, with the three successive approximation devices staggered to receive one out of every three inputs.

[0025] The above has described matched unit cell capacitors, but it should also be understood that other capacitors could be used. Conventional capacitors which are not matched in this way can be used. In addition, the capacitors can be scaled relative to one another by some amount, e.g. in powers of two.

[0026] All such modifications are intended to be encompassed within the following claims.